REMARKS

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold type.

Claim 27 and 31 are objected to because of the following informalities: Claim 31 now being dependent upon claim 30 provides for proper antecedent basis for the term "the filtered voltage signal", however, claim 30 and claim 1 which claim 30 depends upon does not provide proper antecedent basis for "the P-type enhancement mode MOSFETs into saturation". Thus it is assumed that applicant meant to set forth "a plurality of P-type enhancement mode MOSFETs into saturation". Claim 27 is dependent upon claim 26, which has been cancelled. It appears to the examiner that applicant meant to amend claim 27 to be dependent upon claim 24 instead? For examiner purposes it will be assumed that claim 27 is dependent upon claim 24. Appropriate correction is required.

Claims have been amended.

Claims 33, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke 6,337,604 (Clarke) in view of Klughart US 5,546,055 (Klughart '055).

The only Figure of Clarke discloses a "circuitry for controlling the oscillating frequency of an oscillator" now just recited as "apparatus" in some of the claims (See column 2, around line 22 of Clarke). The circuitry/apparatus of Clarke has a plurality of on-chip capacitors Cl-C6 (Note that the capacitors are part of the "integrated circuit" 3 and thus are on-chip capacitors. In fact note the term "ON-CHIP COMPONENTS" as recited by the only Figure of Clarke.). Each of these capacitors is independently selectable by a control signal DO-D5, and each of these capacitors provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (Again see column 2, around line 22 of Clarke).

Clarke is silent on the composition of the on-chip capacitors Cl-C6. Figure 9 of Klughart '055 discloses the use of on-chip n-depletion MOSFET load capacitors 1230 and 1232 whose source and drain are clearly connected together as is clearly illustrated. Also note that the source/drain terminal of each of these capacitors is the terminal that is connected to ground in Klughart '055.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip n-depletion MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors C1-C6 of Clarke wherein each of these capacitors C1-C6 has a terminal connected to ground because, as the Clarke reference is silent as to

the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip n-depletion MOSFET capacitors as recited by Klughart '055 for the capacitors of Clarke.

As noted in the previous office actions, the only Figure of Clarke discloses an electronic device comprising a real time clock, i.e., oscillator, for generating a system time signal "CLK OUT 5 " (See the only Figure and column 2, around line 20). The real time clock has a digitally tunable oscillator (Note the use of the set of shift registers 21) for digitally adjusting the operating frequency of the real time clock to speed up or slow down the system time signal (See column 3, around line 45). Clarke also has a memory device 21 for storing the data representing a configuration of the digitally adjusted tunable oscillator. Claim 35 merely recites that the device generates a time signal based on the oscillating frequency of the oscillator. The "CLK OUT 5" is a time signal that is clearly based on the oscillating frequency of the oscillator in Clarke. Note that the examiner must give the broadest reasonable interpretation consistent with the specification. (See MPEP 904.01).

Clarke does not disclose or suggest "a low pass filter to provide a bias voltage to bias the drain and source of at least one of the plurality of P-type MOSFET capacitors, the low pass filter allowing high frequency noise from a power supply to pass to ground so that the bias voltage has reduced high frequency noise," as recited in amended claim 33. Clarke merely shows capacitors, each having two ends, in which one end is connected to ground and the other end is connected to a Vbias voltage through a resistor (see only figure of Clarke).

What is missing in Clarke is also not disclosed or suggested in Klughart '055, which shows n-depletion MOSFET capacitors C1 and C2 (1230 and 1232), each having drain and source nodes that are connected to ground, and a gate node that is connected to a node of a crystal oscillator 1228 (see figure 9 of Klughart '055).

Claims 1-3, 5, 30, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke 6,337,604 (Clarke) in view of Ochiai et al. US 4,851,792 (Ochiai) and Klughart US 5,546,055 (Klughart '055).

...

Claims like claim 1 has been previously amended to recite a bias circuit to provide a "substantially constant voltage signal" to the bias at least one of the plurality of capacitors. The voltage signal Vbias is considered by Clarke to be a bias voltage signal and it is applied to the capacitors C1-C6 via a resistor element 33 as is clearly illustrated by Clarke. Thus this voltage signal of Clarke is considered to be a "substantially constant voltage". Note that applicant has not provided for a specific definition of "substantially constant voltage signal" in the specification. As noted in previous office actions this bias voltage signal

of Clarke must be "substantially constant" otherwise the operating point of transistors Q1, 43, 44 and Q5 would change and thus not achieving a stable oscillator as disclosed by Clarke. Also given the breath of the term bias and applicant has not provided any specific definition for such the voltage Vcc of Clarke is considered to be a bias voltage signal that is considered to be "substantially constant voltage". Again an erratic voltage V, would not result in a stable oscillator, which is disclosed by Clarke. The voltage signal Vcc must be "substantially constant". Note that Vcc is applied to the capacitors via unmarked resistors as is clearly illustrated by Clarke. However, alternatively Figure 8(a) of Ochiai discloses a biasing arrangement for the capacitors of an oscillator and is configured such that the bias voltage VB of the capacitor 14 "remains constant" (See column 5 around line 61 of Ochiai). This as recognized by Ochiai allows for the oscillation frequency to remain constant. It is conventionally known that changes of bias to a MOS type capacitor including MOSFET based MOS capacitors will cause changes in its capacitance much like a pin arrangement. It is the teaching of Clarke to have capacitors C1-C6 to be capacitors having discrete i.e. non-changing values. Clarke obtains the change in capacitance by switching these capacitors of discrete values in and out of the circuit. Clarke shows and describes no means by which the individual capacitances of these capacitors are changed.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the oscillator arrangement of Clarke and Klughart '055 with a bias arrangement that keeps the necessary bias voltage of the capacitor elements constant so as to prevent the individual capacitance elements from varying in capacitance and thus preventing an undesirable drift in oscillator frequency as taught by Ochiai.

As discussed above, neither Clarke nor Klughart '055 discloses or suggests "a low pass filter to provide a bias voltage to bias the drain and source of at least one of the plurality of P-type MOSFET capacitors, the low pass filter allowing high frequency noise from a power supply to pass to ground so that the bias voltage has reduced high frequency noise," as recited in amended claim 1.

What is missing in Clarke and Klughart is also not disclosed or suggested in Ochiai, which merely shows a floating gate MOS variable capacitor 14 (col. 2, line 64).

Claims 1-4, 30-32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke 6,337,604 (Clarke) in view of Ochiai et al. US 4,851,792 (Ochiai) and Klughart US 5,801,411 (Klughart '411).

...
Figure 9b of Klughart '411 discloses the use of on-chip p-enhancement MOSFET capacitor 32 whose source and drain are clearly connected together as "common " i.e. conventional (See column 7, around line 18). Also note that the source/drain terminal of each of these capacitors is the terminal that is

> **connected to ground in Klughart '411. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted on-chip p-enhancement MOSFET load capacitors wherein the source/drain terminal of each of the individual capacitors is the terminal that is connected to ground in place of the generic capacitors C1 -C6 of Clarke wherein each of these capacitors C1 -C6 has a terminal connected to ground because, as the Clarke reference is silent as to the exact composition of the capacitors one of ordinary skill in the art would have been motivated to use any art-recognized equivalent capacitor such as the well-known on-chip p-enhancement MOSFET capacitors as recited by Klughart '411 for the capacitors of Clarke.**
>
> **...**
>
> **Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the oscillator arrangement of Clarke and Klughart '411 with a bias arrangement that keeps the necessary bias voltage of the capacitor elements constant so as to prevent the individual capacitance elements from varying in capacitance and thus preventing an undesirable drift in oscillator frequency as taught by Ochiai.**

As discussed above, neither Clarke nor Ochiai discloses or suggests "a low pass filter to provide a bias voltage to bias the drain and source of at least one of the plurality of P-type MOSFET capacitors, the low pass filter allowing high frequency noise from a power supply to pass to ground so that the bias voltage has reduced high frequency noise," as recited in amended claim 1.

What is missing in Clarke and Ochiai is also not disclosed or suggested in Klughart '411, which shows using a current source to bias a drain-source connected N-type MOSFET capacitor (Fig. 26).

> **Claims 13, 15, 16, 24, 25, and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horn "Basic Electronics Theory" 4th Edition pp 377-378 and pp 454-465 in view of Clarke US 6,337,604 (Clarke).**
>
> **Beginning on page 420 of Horn, Horn describes the basic well-known structure of a computer. Horn describes the speed of the computer that as known by those of ordinary skill this is describing the oscillator or "real time clock" that is inherently within the computer. Also within a computer, computers inherently have a system time signal that represents at least one of hour, minute and second, and this is the clock signal itself. For example 100 clock pulses will represent X number of seconds, etc. Note that software will take this and display on a monitor the hours, minutes and seconds of a day but the claims only requires a system time signal that represents at last one of hour, minute and second. Horn is silent on the specifics of the oscillator or real time clock or just clock.**

> **The single Figure of Clarke discloses a circuitry for controlling the oscillating frequency of an oscillator (See column 2, line 22), the circuitry having a plurality of on-chip capacitors C1-C6, each of which is independently selectable by a control signal DO-D5, and each of which provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22).**
>
> **The single Figure of Clarke also discloses an electronic device comprising a real time clock, i.e., oscillator, for generating a system time signal "CLK OUT 5" (See the only Figure and column 2, around line 20), the real time clock having a digitally tunable oscillator (Note the use of set of shift registers 21) for digitally adjusting an operating frequency of the real time clock to speed up or slow down the system time signal (See column 3, lines 45), and a memory device 21 for storing data representing a configuration of the digitally adjusted tunable oscillator.**
>
> **Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the conventional real time clock/oscillator circuit of Clarke for the oscillator/real time clock/clock of Horn because, as the reference is silent as the exact oscillator/clock circuit employed one of ordinary skill in the art would have been motivated to use any art-recognized equivalent switch such as the well-known, conventional oscillator/clock circuit of Clarke. One of ordinary skill in the art also would have been additionally motivated to make the combination because Clarke teaches that the real time clock can be adjusted i.e. calibrated and thus it is advantageous to make a clock adjustable so that one can adjust the clock frequency to obtain the desired frequency as taught by Clarke. Note that Clarke contains a processor and set of control signals that adjusts the frequency of the real time clock of Clarke is stored in a register 21.**
>
> **Also note that since Clarke senses the real time clock and Horn clearly uses this real time clock to develop the system time signal the data processing unit of Clarke processes data based on the system time signal. In other words the system time signal and the real time clock signal are related and sensing one is in effect sensing the other and thus it is an obvious consequence that the data processing unit of Clarke processes data based on the system time signal. The examiner must give the broadest reasonable interpretation to the claims consistent with the specification.**

The examiner appears to contend that it would have been obvious to use a clock circuit of Clarke for generating an inherent system time signal in the computer of Horn. The applicant disagrees. Horn merely describes increasing the system clock to increase computer operating speed, which has nothing to do with adjustment "of the real time clock to speed up or slow down the system time signal," as recited in claim 13. What Clarke discloses is a "standard clock signal" (col. 2:20), and nowhere does Clarke disclose or suggest that the standard clock signal can be used as a real time clock for generating a system time signal.

The examiner appears to take the position that because Clarke does not say what the standard clock signal is used for, the standard clock signal can be used for any purpose, whether Clarke makes such a suggestion or not. The applicant notes that the clock circuit disclosed in Clarke would not be suitable for use as a real time clock circuit in the computer of Horn. Clock circuits are sensitive to noise. The system clock of a computer typically runs several megahertz or gigahertz (for example, the 386 and 486 microprocessors disclosed in Horn operates at or above 16 MHz). If the clock circuit of Clarke were used in the computer of Horn to generate system time, high frequency noise from other components of the computer would couple to the clock circuit of Clarke through the power supply voltage signal Vcc, causing glitches and affecting the accuracy of the system time.

The applicant discovered that an adjustable real time clock circuit having drain-source connected P-type MOSFET capacitors can be implemented when a low pass filter is used to generate a bias voltage to bias the source and drain nodes of the MOSFET capacitors. The low pass filter filters the high frequency noise in the power supply, reducing the high frequency noise in the bias voltage. Without the applicant's invention, Clarke's clock circuit would not function well as a real time clock circuit in the computer of Horn, and thus there would be no suggestion or motivation to use Clarke's clock circuit in Horn's computer.

Claims 16 and 24 are patentable for at least the same reasons as claim 13.

The dependent claims are patentable for at least the same reasons as the claims on which they depend.

Enclosed is a $450.00 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050, referencing attorney docket 10559-650001.

Respectfully submitted,

Date: 3/18/2005

Rex Huang

Rex Huang* for
David L. Feigenbaum, Reg. No. 30,378

PTO Customer No. 26161
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

** See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 CFR § 10.9(b).*

20962559.doc